REMARKS

Summary Of Office Action

Claims 1-53 were pending in this application.

Claims 2, 21, 23, 24, 26, 29, 30, 31, and 40 were objected to for containing various informalities.

Claims 12, 41, 42, and 53 were rejected under 35 U.S.C. § 102(a) as being anticipated by Olarig et al. U.S. Patent No. 6,134,638 (hereinafter "Olarig").

Claims 1-3, 5-7, 9-10, 43-45, 47-49, and 51 were rejected under 35 U.S.C. § 103(a) as being obvious from Olarig in view of Ikeda, U.S. Patent No. 6,487,086 (hereinafter "Ikeda") and Schwartz U.S. Patent No. 4,468,729 (hereinafter "Schwartz").

Claims 4, 8, 11, 46, 50, and 52 were rejected under 35 U.S.C. § 103(a) as being obvious from Olarig, Ikeda, and Schwartz, further in view of Johnson et al. U.S. Patent No. 5,577,236 (hereinafter "Johnson") and Chang et al. U.S. Patent No. 5,610, 543 (hereinafter "Chang").

Claims 13-15, 17-19, 25-27, 30-32, 34-36, 38, and 39 were rejected under 35 U.S.C. § 103(a) as being obvious from Olarig in view Stevens et al. U.S. Patent No. 6,226,729 (hereinafter "Stevens") and Ikeda.

Claims 16, 20, 28, 29, 33, and 37 were rejected under 35 U.S.C. § 103(a) as being obvious from Olarig, Stevens, and Ikeda further in view of Johnson and Chang.

Claims 21 and 24 were rejected under 35 U.S.C. § 103(a) as being obvious from Olarig, Stevens, and Ikeda, further in view of Hartwell U.S. Patent No. 6,724,850 (hereinafter "Hartwell").

Claims 22 and 23 were rejected under 35 U.S.C. § 103(a) as being obvious from Hartwell, Olarig, Stevens, and Ikeda, further in view of Johnson and Chang.

Claim 40 was rejected under 35 U.S.C. § 103(a) as being obvious from Olarig, Hartwell, and Johnson further in view of Chang.

Summary Of Applicant's Reply

Applicant has amended claims 1-3, 9, 11-13, 21, 23, 24-26, 29-32, 38, 40, 41, 43, 45, and 51-53 to more particularly define the invention. Applicant has canceled claim 42 without prejudice.

No new matter would be added by the proposed amendments and all of the amendments are fully supported by the original specification.

Reconsideration of this application in view of the proposed amendments and the following remarks is respectfully requested.

Objections to Claims 2, 21, 23
24, 26, 29, 30, 31, and 40

The Examiner objected to claims 2, 21, 23, 24, 26, 29, 30, 31, and 40 for containing various informalities. Applicant has amended claim 2, 21, 23, 24, 26, 29, 30, 31, and 40 and respectfully submits that these amended claims are not objectionable. Accordingly, applicant respectfully requests that the objections to claims 2, 21, 23, 24, 26, 29, 30, 31, and 40 be withdrawn.

Rejection of Claims
Under 35 U.S.C. § 102(a)

Claims 12, 41, 42, and 53 were rejected under 35 U.S.C. § 102(a) as being anticipated by Olarig. This rejection is respectfully traversed.

Amended independent claims 12, 41, and 53 are directed toward a method, a memory controller, and an

apparatus, respectively, for selecting an operating speed of a memory module interface. Multiple clock signals are generated at different frequencies to provide selectable operating speeds for the memory module interface. The number of memory modules is counted and a running tally of the number of memory modules is maintained based on the counting. Information is obtained that includes at least the speed grade of the memory module. Based on at least a final tally of the number of memory modules and the obtained information, only one of the multiple clock signals is selected to provide the operating speed of the memory module interface.

Olarig refers to a memory controller supporting multiple DRAM circuits that all may operate at different frequencies. Upon initialization, the computer system determines the type of DRAM circuits present and provides status information to the memory controller which, in response, generates multiple clock signals with appropriate frequencies. The multiple clock signals are respectively applied to the SDRAM memory devices which "may operate at different frequencies appropriate for each SDRAM device." Olarig, column 3, lines 10-16 (emphasis added).

However, Olarig does not show counting the number of memory modules, maintaining a running tally of the number of memory modules, or selecting only one of the multiple clock signals based at least on the final tally of the memory modules and the speed grade of the memory modules, as required by amended independent claims 12, 41, and 53.

Accordingly, applicant respectfully requests that the rejection of independent claims 12, 41, and 53 be withdrawn.

Rejections of Claims
Under 35 U.S.C. § 103(a)

Claims 1-3, 5-7, 9-10, 43-45, 47-49, and 51 were rejected under 35 U.S.C. § 103(a) as being obvious from Olarig, Ikeda, and Schwartz. Claims 4, 8, 11, 46, 50, and 52 were rejected under 35 U.S.C. § 103(a) as being obvious from Olarig, Ikeda, and Schwartz, further in view of Johnson and Chang. Claims 13-15, 17-19, 25-27, 30-32, 34-36, 38, and 39 were rejected under 35 U.S.C. § 103(a) as being obvious from Olarig further in view Stevens and Ikeda. Claims 16, 20, 28, 29, 33, and 37 were rejected under 35 U.S.C. § 103(a) as being obvious from Olarig, Stevens, and Ikeda further in view of Johnson and Chang. Claims 21 and 24 were rejected under 35 U.S.C. § 103(a) as being obvious from Olarig, Stevens, and Ikeda, further in view of Hartwell. Claims 22 and 23 were rejected under 35 U.S.C. § 103(a) as being obvious from Hartwell, Olarig, Stevens, and Ikeda, further in view of Johnson and Chang. These rejections are respectfully traversed.

I. Rejections of Independent Claims 1, 9, 43 and 51

Independent claims 1, 9, 43, and 51 are directed toward methods and apparatus for selecting an operating speed of a memory module interface. The number of memory modules is counted and a running tally of the number of memory modules is maintained based on the counting. Multiple clock signals are generated at different frequencies to provide selectable operating speeds for the memory module interface. Based on at least a final tally of the number of memory modules, only one of the multiple clock signals is selected to provide the operating speed of the memory module interface. Claims 9 and 51 further specify that information is obtained from the memory modules, including at least one characteristic of the

memory modules, and the selection of the clock signal is based on at least the final tally and the obtained information.

The Examiner's position in this rejection appears to be that (1) Olarig shows generating multiple clock signals at different frequencies to provide selectable operating speeds and selecting one of said operating speeds, (2) Ikeda also shows generating multiple clock signals at different frequencies to provide selectable operating speeds and selecting one of said operating speeds based at least on a final tally of the number of memory modules, and (3) Schwartz shows counting the number of memory modules and keeping a running tally of the number of memory modules, and that the combination of these three references makes applicant's claims unpatentable. Applicant respectfully disagrees with the Examiner's position.

Applicant respectfully submits that neither Olarig nor Ikeda nor Schwartz shows or suggests all of the elements of applicant's independent claims. Further, whether or not the combination of these references are proper, the combination of features which these references cumulatively contribute also falls short of showing or suggesting applicant's claimed invention.

Olarig does not show or suggest selecting only one clock signal from multiple clock signals to provide an operating speed. Rather than selecting one clock signal, Olarig uses the multiple generated clock signals to provide multiple operating speeds for each of the different memory devices in order to "optimize the performance of each memory device by performing transactions at the fastest possible speed with each memory circuit." Olarig, column 2, lines 63-65. Thus, Olarig does not show or suggest applicant's claimed feature of selecting only one of the

multiple clock signals to provide the operating speed of the memory module interface.

Further, Olarig teaches away from selecting only one clock signal from the multiple generated clock signals. While discussing the background of the alleged invention, Olarig refers to previous systems that contain memory modules that are capable of running at different speeds. These previous systems would run "the computer system at the speed of the slowest memory device." Olarig, column 2, lines 53-54. Olarig refers to an improvement of these systems, namely "a computer system that is capable of implementing memory devices with different operating speeds." Id., lines 60-61. Thus, Olarig teaches away applicant's claimed feature of selecting only one of the multiple clock signals to provide the operating speed of the memory module interface.

Ikeda also does not show or suggest applicant's claimed feature of selecting only one of multiple clock signals to provide the operating speed of the memory module interface. Further, Ikeda does not show or suggest selecting only one clock signal based on a final tally of the number of memory modules, as required by applicant's claims.

In the "Background of the Invention," Ikeda mentions that in some systems the frequency of the memory control clock is limited by the number of memory modules connected to parallel memory sockets. For example, when the control clock frequency is 100 MHz only four memory modules may be connected and when the control clock frequency is 133 MHz only two memory modules may be connected. See, Ikeda, column 1, lines 45-62. Ikeda refers to improved contact terminals for memory modules that reduce this problem by improving the impedance matching between the main board and the memory modules. Ikeda does not show or suggest generating multiple

clock signals at different frequencies or selecting only one of the multiple clock signals based on a final tally of the number of memory modules. In contrast, Ikeda shows that improving impedance matching in contact terminals may permit the use of high frequency clock signals with multiple memory modules.

Schwartz also does not show or suggest these elements of applicant's independent claims. Schwartz refers to an automatic memory module address assignment system for available memory modules, in which the number of memory modules in the system are counted. However, as the Examiner concedes, Schwartz does not show or suggest selecting only one of multiple clock signals to provide the operating speed of the memory module interface based on a final tally of the number of memory modules.

Accordingly, whether taken alone or in combination, Olarig, Ikeda, and Schwartz do not show or suggest selecting only one of multiple clock signals to provide the operating speed of the memory module interface based on a final tally of the number of memory modules, as required by applicant's independent claims 1, 9, 43, and 51.

Further, while the Examiner has attempted to provide motivations to combine these references, the Examiner has not shown any motivation to combine these three references in a manner that would show or suggest each of the elements of applicant's claims.

In support of the combination of Olarig and Ikeda, the Examiner contends that "[o]ne of ordinary skill in the art would have been motivated to make such a combination as it provides a way to account for limitations in signal transmissions caused by reflections and distortions in conventional memory structures." Office Action, page 5.

However, this alleged teaching of Ikeda does not provide motivation to select only one clock signal of multiple clock signals based on a final tally of the number of memory modules. Instead, the Examiner has merely provided an alleged motivation to use the memory contact terminals of Ikeda in Olarig to reduce reflections and distortions to maximize memory operating speeds.

In support of the combination of Olarig and Schwartz, the Examiner contends that "[o]ne of ordinary skill in the art would have been motivated to make such a combination as it provides a way to ensure sufficient memory capacity for proper operation." Office Action, pages 5-6. However, this alleged teaching of Schwartz does not provide motivation to count the number memory modules in order to select only one clock signal of multiple clock signals based on a final tally of the number of memory modules. Instead, the Examiner has merely provided an alleged motivation to use the teaching of Schwartz to count the number of memory modules in Olarig in order to determine the total capacity of the installed memory.

Accordingly, there is no motivation to combine Olarig, Ikeda, and Schwartz in the manner suggested by the Examiner.

Moreover, applicant respectfully submits that the Examiner has employed hindsight reconstruction in combining the references. With the knowledge of applicant's novel system for selecting only one of multiple clock signals to provide the operating speed of the memory module interface based on a final tally of the number of memory modules, particular features of the prior art were identified for use in rejecting applicant's invention. This technique has long been held invalid by the courts at creating a *prima facie* case

of obviousness. See In re Fine, 5 USPQ2d at 1600. ("One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.").

The Examiner has used applicant's own invention as a bridge between Olarig, Ikeda, and Schwartz, selecting isolated features of their systems in an attempt show all of the features of applicant's claims. In doing so, the Examiner has demonstrated mere hindsight reconstruction, the very "syndrome" that the requirement for objective evidence is designed to combat, and the rejection is therefore insufficient as a matter of law. See In re Dembiczak, 50 USPQ2d at 1617-1618.

Accordingly, applicant respectfully requests that the rejection of independent claims 1, 9, 43, and 51 be withdrawn.

II. Rejections of Independent Claims 11 and 52

Independent claims 11 and 52 are directed toward a method and an apparatus for selecting an operating speed of a memory module interface. Multiple clock signals are generated at different frequencies to provide selectable operating speeds for the memory module interface. Information is obtained from the memory modules, including at least the number of components in each memory module. Based on a final tally of the number of memory modules, only one of multiple clock signals is selected to provide the operating speed of the memory module interface.

The Examiner concedes that Olarig, Ikeda, and Schwartz do not show or suggest obtaining information from the memory modules including at least the number of components in

the memory module and selecting only one clock signal of multiple clock signals based on this information. In response to this deficiency in Olarig, Ikeda, and Schwartz, the Examiner suggests combining Olarig, Ikeda, and Schwartz with Johnson and Chang.

Johnson refers to a memory controller for reading data from synchronous RAM. In Johnson, a sampling clock provides an assortment of sampling clock signals that duplicate the system clock signal with various delays. In response to the number of memory modules present or the number of memory circuits in each memory module, the clock selector selects one of the delayed sampling clock signals. However, Johnson does not show or suggest generating multiple clocks at different frequencies. Instead, Johnson refers to generating multiple clocks at the same frequency, but with different amounts of delay.

In response to this deficiency in Johnson, the Examiner suggests combining Johnson with Chang. Chang refers to a delay-locked loop system for detecting the phase difference between two signals having different frequencies. The Examiner is attempting to use Chang to show that generating and selecting a clock signal based on the frequency of the clock signal is the same as generating and selecting a clock signal based on the phase delay of the clock signal. More particularly, the Examiner contends that "one of ordinary skill in the art would have selected a lower frequency instead of delaying the clocks to increase the data valid window in order to reduce power consumption." Office Action, page 7.

Applicant respectfully submits that the combination of Olarig, Ikeda, Schwartz, Johnson, and Chang does not show all of the elements of applicant's independent claims 11 and 52. In particular, the combination of these references

does not show obtaining information from the memory modules including at least the number of components in the memory module and selecting only one of multiple clock signals, generated at different frequencies, to provide the operating speed of the memory module interface.

Further, the Examiner has not provided sufficient motivation to combine all of these references in the manner suggested. In particular, the Examiner has not even attempted to provide any motivation to combine Johnson with Olarig, Ikeda, and Schwartz. Then, the Examiner has attempted to combine Chang with Johnson in spite of the fact the Chang does not relate to the field of memory module interfaces and that the only motivation supplied by the Examiner (i.e., increased data valid windows and reduced power consumption) relate to the system of Chang (delay-locked loops) and not to Johnson, the remaining references, or applicant's independent claims.

Moreover, applicant respectfully submits that the Examiner has employed hindsight reconstruction in combining the references. The Examiner has used applicant's own invention as a bridge between Olarig, Ikeda, Schwartz, Johnson, and Chang selecting isolated features of their systems in an attempt show all of the features of applicant's claims.

Accordingly, applicant respectfully requests that the rejection of independent claims 11 and 52 should be withdrawn.

III. Rejections of Independent Claims 13, 25, 26, 30, 31 and 38

Independent claims 13, 25, 26, 30, 31, and 38 are directed toward computer systems and memory controllers for selecting an operating speed of a memory module interface. The number of memory modules is counted and a running tally of

the number of memory modules is maintained based on the counting. Multiple clock signals are generated at different frequencies to provide selectable operating speeds for the memory module interface. Based on a final tally of the number of memory modules, only one of multiple clock signals is selected to provide the operating speed of the memory module interface. Claims 26 and 38 further specify that information is obtained from the memory modules, including at least one characteristic of the memory modules, and the selection of the clock signal is based on at least the final tally and the obtained information.

As previously discussed with respect to independent claims 1, 9, 43, and 51, Olarig and Ikeda taken alone or in combination do not show or suggest counting the number of memory modules, maintaining a running tally of the number of memory modules based on the counting, or selecting one of multiple clock signals to provide the operating speed of the memory module interface based on at least a final tally of the number of memory modules. In response to these deficiencies in Olarig and Ikeda, the Examiner suggests combining Olarig and Ikeda with Stevens.

Stevens refers to a method for configuring or initializing a memory device. During configuration or initialization, a clock generator is started in the memory controller. The frequency of the single generated clock signal is selected by "determining a channel frequency at which all [memory modules] may operate" (Stevens, column 13, lines 43-45).

In support of this rejection, the Examiner contends that Stevens shows generating multiple clock frequencies and selecting one of the clock frequencies based on a final tally

of the number of memory modules. Applicant respectfully submits that Stevens makes no such showing.

In support of the contention that Stevens shows generating multiple frequencies the Examiner cites two sources (1) Stevens, column 13, lines 41-49 and (2) Applicant's Remarks dated November 16, 2004, page 3. Neither of these sources support the Examiner's contention.

> Stevens states, in relevant part, that:
>
> The clock generator is block 608. This operation may be accomplished by software querying the SPD data of every RIMM module present on the motherboard and determining a channel frequency at which all RIMMs may operate. Stevens, column 13, lines 21-45 (emphasis added).

Thus, Stevens refers to a system that generates a single channel frequency and not multiple channel frequencies.

Applicant's Remarks dated November 16, 2004 were responsive the Office Action of August 19, 2004. Applicant stated, in relevant part, that:

> Stevens, as the Examiner correctly acknowledges, does not disclose or suggest generating multiple clocks at different frequencies to provide the selectable operating speeds. Lines 9-12 (emphasis added).

Thus, to the contrary of the Examiner's contention, applicant's have maintained throughout prosecution that Stevens does not show or suggest generating multiple clock frequencies.

In fact, the Examiner in the Office Actions of August 19, 2004 and March 4, 2005 conceded that "Stevens did not disclose explicitly generating multiple clock frequencies." Office Action of August 19, 2004, page 3, line 3 and Office Action of March 4, 2005, page 3, line 5.

Accordingly, applicant submits that the Examiner has failed to support the contention that Stevens shows generating multiple clock frequencies.

Applicant also respectfully submits that Stevens does not show or suggest selecting only one of the multiple clock signals based on a final tally of the number of memory modules. As described above, Stevens only refers to selecting a clock frequency "at which all RIMMs may operate." Stevens, column 13, lines 44-45. Thus, Stevens only selects a single clock frequency based on the speed of the memory modules and not based on a final tally of the number of memory modules.

Moreover, Stevens and Olarig are incompatible and may not be combined in the manner suggested by the Examiner. Stevens and Olarig refer to contrary techniques for selecting clock speeds in memory controller systems containing memory devices that operate at different speeds. Stevens "determin[es] a [i.e., one] channel frequency at which all [memory devices] may operate." Stevens, column 13, lines 43-45. In contrast, Olarig "generates multiple clock signals with appropriate frequencies for use by the SDRAM memory devices." Olarig, abstract, lines 3-5. Thus, Stevens generates a single clock signal of appropriate frequency for the memory controller while Olarig generates a different clock signal for each memory device. Accordingly, the techniques of Stevens and Olarig are incompatible.

Thus taken alone or in combination, neither Olarig nor Stevens nor Ikeda shows or suggests applicant's claimed feature of generating multiple clock signals to provide selectable operating speeds for the memory module interface and selecting only one of the multiple clock signals to provide the operating speed for the memory module interface based on a final tally of the number of memory modules.

Moreover, the Examiner has not provided sufficient motivation to combine Olarig, Stevens, and Ikeda in the manner suggested and has employed hindsight reconstruction in using applicant's own invention as a bridge between Olarig, Stevens, and Ikeda by selecting isolated features of their systems in an attempt show all of the features of applicant's claims.

Accordingly, applicant respectfully requests that the rejection of independent claims 13, 25, 26, 30, 31, and 38 be withdrawn.

IV. Rejections of Independent Claims 21, 23, 24, 29 and 40

The Examiner asserts that the combination of Olarig, Stevens, and Ikeda further in view of Hartwell shows all of the elements of applicant's amended independent claims 21 and 24. Applicant respectfully disagrees with the Examiner's assertion. The application of Hartwell for the alleged teaching of the additional elements of claims 21 and 24 does not make up for the deficiencies of Olarig, Stevens, and Ikeda. In particular, for at least the reasons discussed above with respect to the patentability of the previously discussed independent claims applicant respectfully submits that independent claim 29 is not rendered obvious by the combination Olarig, Stevens, and Ikeda further in view of Johnson and Chang.

The Examiner asserts that the combination of Olarig, Stevens, and Ikeda further in view of Johnson and Chang shows all of the elements of applicant's amended independent claim 29. Applicant respectfully disagrees with the Examiner's assertion. The application of Johnson and Chang for the alleged teaching of the additional elements of claim 29 does not make up for the deficiencies of Olarig, Stevens, and Ikeda. In particular, for at least the reasons discussed

above with respect to the patentability of the previously discussed independent claims applicant respectfully submits that independent claim 29 is not rendered obvious by the combination Olarig, Stevens, and Ikeda further in view of Johnson and Chang.

The Examiner asserts that the combination of Hartwell, Olarig, Stevens, and Ikeda further in view of Johnson and Chang shows all of the elements of applicant's amended independent claim 23. Applicant respectfully disagrees with the Examiner's assertion. The application of Johnson and Chang for the alleged teaching of the additional elements of claim 23 does not make up for the deficiencies of Hartwell, Olarig, Stevens, and Ikeda. In particular, for at least the reasons discussed above with respect to the patentability of the previously discussed independent claims applicant respectfully submits that independent claim 23 is not rendered obvious by the combination Hartwell, Olarig, Stevens, and Ikeda further in view of Johnson and Chang.

The Examiner asserts that the combination of Olarig, further in view of Hartwell, Johnson, and Chang shows all of the elements of applicant's amended independent claim 40. Applicant respectfully disagrees with the Examiner's assertion. The application of Hartwell, Johnson, and Chang for the alleged teaching of the additional elements of claim 40 does not make up for the deficiencies of Olarig. In particular, for at least the reasons discussed above with respect to the patentability of the previously discussed independent claims, applicant respectfully submits that independent claim 40 is not rendered obvious by the combination Olarig further in view of Hartwell, Johnson, and Chang.

Accordingly, applicant respectfully requests that the rejection of independent claims 21, 23, 24, 29 and 40 should be withdrawn.

V. Rejections of Dependent Claims

For at least the reasons discussed above with respect to independent claims 1, 9, 11-13, 21, 23-26, 29-31, 38, 40, 41, 43, and 51-53, dependent claims 2-8, 10, 14-20, 22, 27, 28, 32-37, 39, and 44-50, which depend directly or indirectly from claims 1, 9, 11-13, 21, 23-26, 29-31, 38, 40, 41, 43, and 51-53 are also not rendered obvious from the various combinations of Olarig, Ikeda, Schwartz, Johnson, Chang, Stevens and Hartwell (i.e., dependent claims are patentable if their independent claim is patentable).

Accordingly, applicant respectfully requests that the rejections of dependent claims 2-8, 10, 14-20, 22, 27, 28, 32-37, 39, and 44-50 be withdrawn.

Contingent Request for Telephonic Interview

If for any reason the Examiner is unable to allow this application based on this Reply, applicants request a telephonic interview with the Examiner before issuance of the next Office Action.

Conclusion

The foregoing demonstrates that claims 1-41 and 43-53 are patentable. This application is therefore in condition for allowance. Reconsideration and allowance are accordingly respectfully requested.

Respectfully submitted,

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